# PRM: A PPMC-Based Rack Monitor

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## Introduction

Rack Monitors have been used at Fermilab to provide networked controls functions in a variety of applications. As technology improves, new versions of Rack Monitors that use this new technology have been implemented. Recently, Motorola announced a new processor module, the PPMC750. This module is designed to operate as a Master PMC module, and VITA currently has a proposed standard for this type of module. The original PMC standard defines a family of slave mezzanine peripheral I/O cards that plug in to a processor baseboard. Traditional architecture uses slave mezzanine I/O modules plugged in to a Master baseboard. The PPMC, Processor-PMC, specification will allow the opposite architecture– a processor PMC module that plugs onto a baseboard containing the custom I/O for the system. This note describes the PRM, a version of Rack Monitor that uses the Motorola PPMC750 processor along with provision to add I/O capability using one additional PMC module and three IP Modules.

## The PPMC750 Card

The Motorola PPMC750 card features a 233 or 350 MHz PowerPC 750 processor, 32 MB of DRAM, 8 MB of flash memory, 1 MB backside cache memory, four 32-bit timers, two watchdog timers, and an RS-232 serial port, all included on a single width PMC module. This module can serve as the the host processor to a group of I/O interfaces built onto a larger baseboard. Development of the baseboard will be much simpler, and testing will be aided, by having an operating cpu board to exercise the various functions.

## PPMC Rack Monitor baseboard

Figure 1 shows a block diagram of a Rack Monitor baseboard designed around the PPMC750. It contains one User PMC slot, three IP sockets, 2 MB of battery-backed Nonvolatile RAM, and an Ethernet adapter. In this design, the PMC slot and the Ethernet adapter both have PCI bus interfaces and will therefore be directly compatible with the PPMC module. An additional PCI-based chip, the PLX9050, connects to PCI bus and converts it to a memory bus architecture to allow connection to the nonvolatile RAM and to the three Altera gate array chips that are included on the baseboard. One of the Altera chips will contain the necessary logic to drive the IndustryPak interface. The other two Altera chips are uncommitted, although they could be used to interface to existing I/O modules used in the Internet Rack Monitor, IRM. Each of the Altera chips has a socket for a serial ROM to load the logic program into the gate array at power-on time, although two of the Altera chips have the option of having their logic downloaded to them by the PPMC processor. Data for this operation may be stored in the onboard nonvolatile RAM.

Figures 2 and 3 show a mechanical arrangement for the PPMC Rack Monitor. These drawings show how existing IRM interface boards and back panel designs can be used. Using this arrangement, the functionality of the IRM can be duplicated in applications where the I/O requirements can be satisfied without the use of VMEbus I/O boards. The only new parts are the baseboard and the PPMC750 itself.

## Software Considerations

Motorola will provide both a ‘bug’ terminal monitor program and the necessary support for porting vxWorks to the PPMC750 board. This, coupled with the DEC 21143 Ethernet adapter, will make the PMC platform appear very similar to the MVME-2400 single board computer that has become the standard for future Fermilab controls applications. This platform will then be able to use normal controls group software. In addition, it should easily fill the requirements of an Epics IOC.

## Compatibility

In addition to a large variety of commercially available mezzanine modules, the PRM can accommodate General Purpose IP modules and the Reconfigureable PMC module, two mezzanine modules designed by Fermilab that have been used for several controls applications. Existing analog and digital transition boards used in the IRM should be directly usable for the PRM. These include the 8-byte digital interface board and the analog interface board containing a 64 channel multiplexed A-D and 8-channel D-A. The 8-channel Swift Digitizer and Quicker Digitizer can also be used.

## Miscellaneous attributes

The functionality of Gate Array 1 is normally fixed and so this chip will be initialized from the attached serial Prom. Because two of the Altera gate arrays are intended to be uncommitted, they will have the option of being downloaded from the processor. Logic to interface to the programming mode pins will be added to Gate Array 1. In this way, the application can choose to use the serial PROM or the parallel download method of initialization for Gate arrays 2 and 3. Gate Arrays 2 and 3 are interconnected via the uncommitted I/O pins on the packages to allow signals, such as clocks and triggers, to be passed between the two gate arrays as needed. If not used, these pins are tri-stated.

Because many accelerator applications require timing information derived from TCLK or MDAT, provision is made for Gate Arrays 2 and 3 to receive these clock signal, and to output signals through external drivers. The outputs may be clocks, gates, or delayed event triggers. Two solid state delay lines are included to aid in decoding and encoding the clock signal.

## Cost

The PRM should cost substantially less than an Internet Rack Monitor because the PPMC750 cost is about half that of an MVME-2400, and a small VMEbus crate is not needed. The actual cost of an application will depend on the number and type of mezzanine modules and transition modules that are used. The basic powered chassis, host board containing the nvRAM, Altera gate arrays, Ethernet adapter, PCI interface chip, Mezzanine connectors, and PPMC750 Processor should be under $2000.

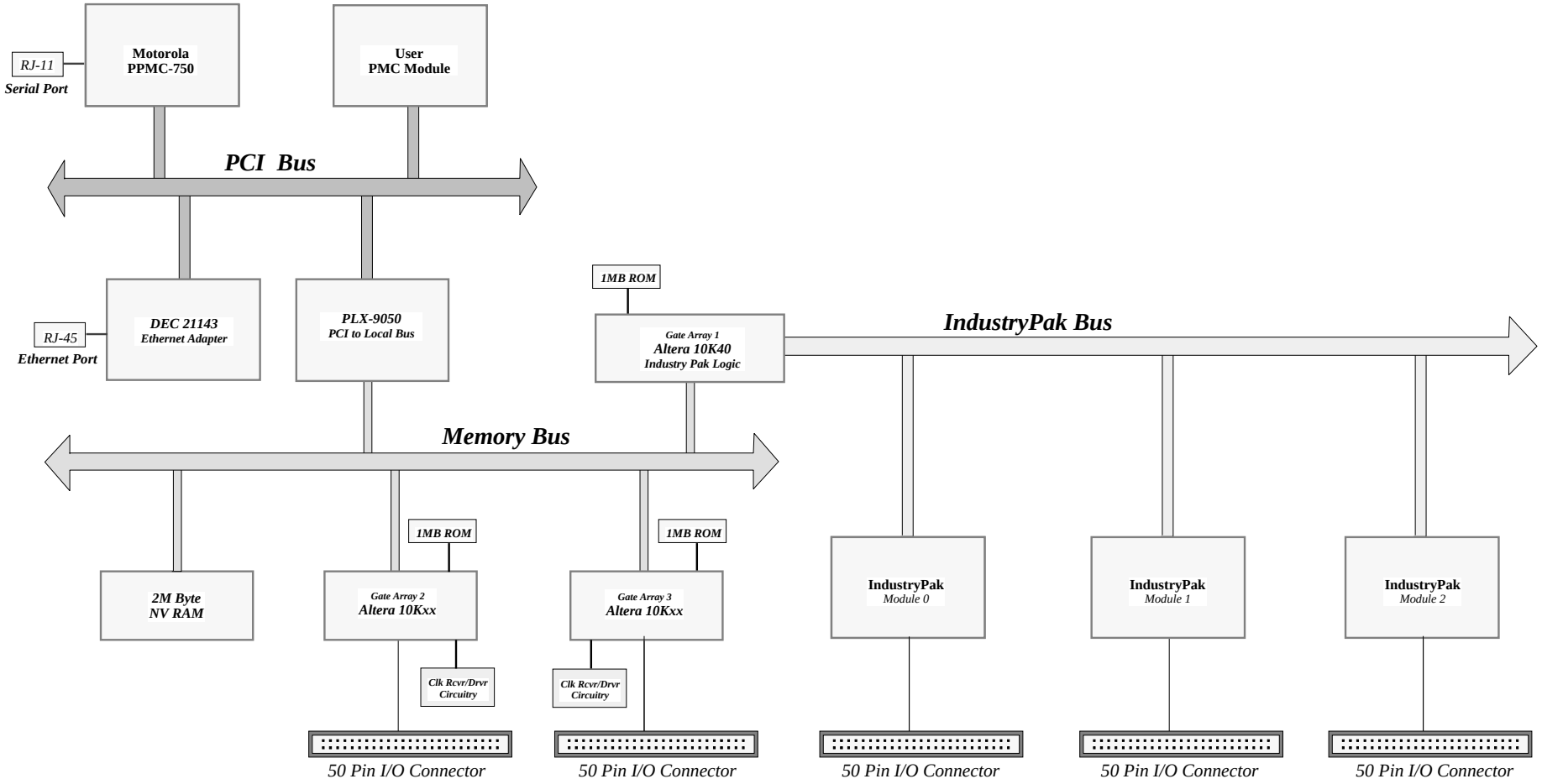


**Figure 1. PRM Host Board**

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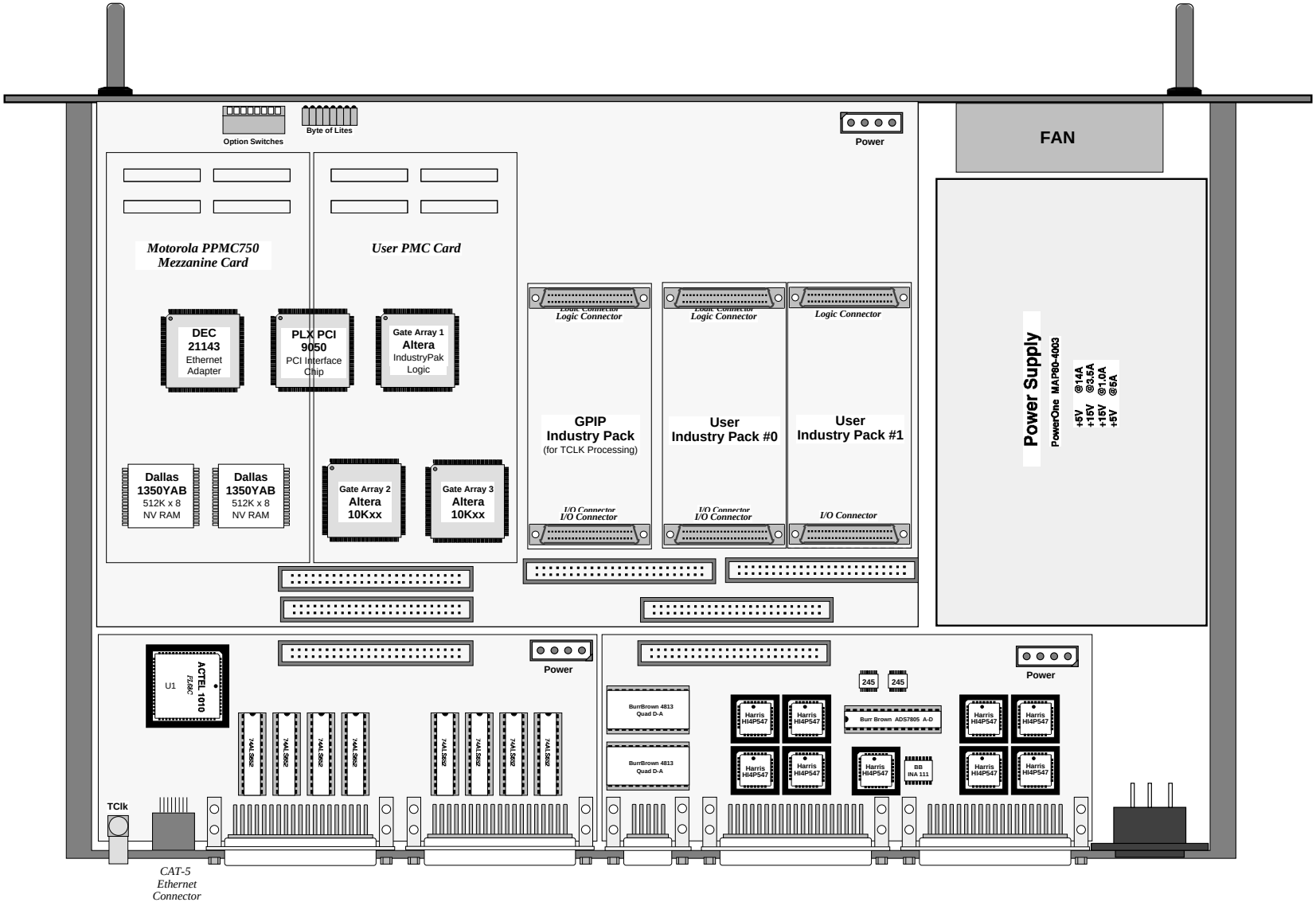


**Figure 2. Plan View of the PRM Rack Monitor**

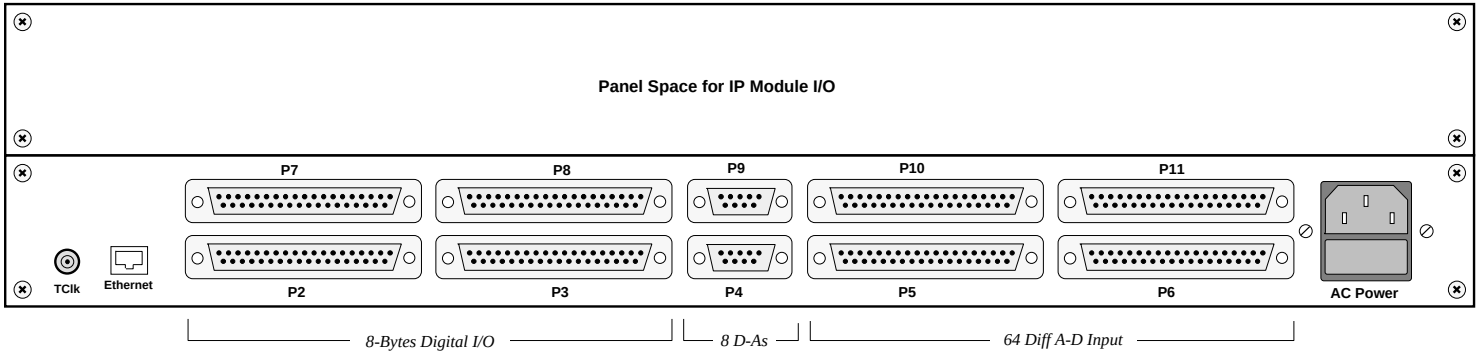


**Figure 3. Back Panel for the PRM**